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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/596,558 | 04/06/2007 | Noriyuki Masago | 40404.40/ko | 7872 |

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| EXAMINER | |
|---|---|
| AUDUONG, GENE NGHIA | |
| **ART UNIT** | **PAPER NUMBER** |
| 2827 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 02/14/2008 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/596,558 | MASAGO ET AL. | |
| | Examiner | Art Unit | |
| | Gene N. Auduong | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *8-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6-19-2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Information Disclosure Statement*

The information disclosure statement (IDS) submitted on June 19, 2006 is being considered by the examiner.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Sawada et al. (US Pat. No. 5,412,601).

Regarding claim 8, Sawada et al. discloses a semiconductor device as in figure 1, comprising: a high voltage production circuit 119 that produces a high voltage; and a high voltage waveform conversion circuit (figure 4, high voltage converter) provided at a subsequent stage of the high voltage production circuit 119 that gradually outputs a high voltage by converting the waveform of the high voltage of the high voltage production circuit 119 (col. 6, lines 66+; col. 14, lines 16+).

Regarding claim 9, Sawada et al. discloses the semiconductor device according to claim 8, further comprising a memory cell (figure 1, memory cells 243…), in which data rewriting is

performed by using a high voltage, wherein the high voltage waveform conversion circuit gradually applies the high voltage to the memory cell (col. 8, lines 29+).

Regarding claim 10, Sawada et al. discloses the semiconductor device according to claim 8, wherein the high voltage waveform conversion circuit comprises a delay circuit that delays the high voltage of the high voltage production circuit, and a voltage conversion switching element that lowers the delayed high voltage by a predetermined value (col. 14, lines 16+; also see figures 2-3).

Regarding claim 11, Sawada et al. discloses the semiconductor device according to claim 9, wherein the high voltage waveform conversion circuit comprises a delay circuit that delays the high voltage of the high voltage production circuit, and a voltage conversion switching element that lowers the delayed high voltage by a predetermined value (col. 14, lines 16+; also see figures 2-3).

Regarding claim 12, Sawada et al. discloses the semiconductor device according to claim 10, wherein the voltage conversion switching element is an N-type MOS transistor in which the high voltage delayed by the delay circuit is input to a gate thereof and the high voltage that has undergone conversion by being lowered by a predetermined value is output from a source thereof (see figures 2-3).

Regarding claim 13, Sawada et al. discloses the semiconductor device according to claim 11, wherein the voltage conversion switching element is an N-type MOS transistor in which the high voltage delayed by the delay circuit is input to a gate thereof and the high voltage that has undergone conversion by being lowered by a predetermined value is output from a source thereof (see figures 2-3).

Regarding claim 14, Sawada et al. discloses the semiconductor device according to claim 8, wherein the high voltage waveform conversion circuit comprises a test signal input section and, when a test signal is input to the test signal input section, the high voltage waveform conversion circuit outputs the high voltage of the high voltage production circuit without converting the waveform (col. 12, lines 42+).

Regarding claim 15, Sawada et al. discloses the semiconductor device according to claim 9, wherein the high voltage waveform conversion circuit comprises a test signal input section and, when a test signal is input to the test signal input section, the high voltage waveform conversion circuit outputs the high voltage of the high voltage production circuit without converting the waveform (col. 12, lines 42+).

Regarding claim 16, Sawada et al. discloses the semiconductor device according to claim 14, wherein the high voltage waveform conversion circuit comprises a delay circuit that delays the high voltage of the high voltage production circuit, a voltage conversion switching element that lowers the delayed high voltage by a predetermined value, and a short-circuit switching element provided parallel to the voltage conversion switching element that short-circuits the voltage conversion switching element when the test signal is input to the test signal input section (col. 14, lines 16+; also see figures 2-3).

Regarding claim 17, Sawada et al. discloses the semiconductor device according to claim 15, wherein the high voltage waveform conversion circuit comprises a delay circuit that delays the high voltage of the high voltage production circuit, a voltage conversion switching element that lowers the delayed high voltage by a predetermined value, and a short-circuit switching element provided parallel to the voltage conversion switching element that short-circuits the

voltage conversion switching element when the test signal is input to the test signal input section (col. 14, lines 16+; also see figures 2-3).

Regarding claim 18, Sawada et al. discloses the semiconductor device according to claim 16, wherein the voltage conversion switching element is an N-type MOS transistor in which the high voltage delayed by the delay circuit is input to the gate thereof and the high voltage that has undergone conversion by being lowered by a predetermined value is output from the source thereof, and the short-circuit switching element is a P-type MOS transistor that is turned ON and outputs the high voltage of the high voltage production circuit as is when the test signal is input to the test signal input section (col. 14, lines 16+; also see figures 2-3).

Regarding claim 19, Sawada et al. discloses the semiconductor device according to claim 17, wherein the voltage conversion switching element is an N-type MOS transistor in which the high voltage delayed by the delay circuit is input to the gate thereof and the high voltage that has undergone conversion by being lowered by a predetermined value is output from the source thereof, and the short-circuit switching element is a P-type MOS transistor that is turned ON and outputs the high voltage of the high voltage production circuit as is when the test signal is input to the test signal input section (figures 2-3).

## ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N. Auduong whose telephone number is (571) 272-1773. The examiner can normally be reached on Monday - Friday from 8:00-4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GA
February 1, 2008

/Gene N. Auduong/
Gene N Auduong
Primary Examiner
Art Unit 2827